REMARKS

I. INTRODUCTION

In response to the Office Action dated September 12, 2005, claims 1 and 11 have been amended. Claims 1-20 remain in the application. Entry of these amendments, and re-consideration of the application, as amended, is requested.

II. CLAIM AMENDMENTS

Applicants' attorney has made amendments to the claims as indicated above. These amendments were made solely for the purpose of clarifying the language of the claims, and were not required for patentability or to distinguish the claims over the prior art.

III. PRIOR ART REJECTIONS

In paragraph (4) of the Office Action, claims 1-6 and 11-16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Huang, U.S. Patent No. 6,442,225 (Huang) in view of Baumgartner et al. U.S. Patent No. 5,712,580 (Baumgartner). However, in paragraph (2), page (5) of the Office Action, claims 7, 8, 9, 10, 17, 18, 19, and 20 were indicated as being allowable if rewritten in independent form to include the base claim and any intervening claims.

Applicants' attorney acknowledges the indication of allowable claims, but respectfully traverses the rejections.

Applicants' claimed invention is patentable over the cited references because it recites elements not taught or suggested by the references. Specifically, the references, taken individually or in combination, do not teach or suggest a clock and data recovery circuit or method where the input data signal is re-timed and de-multiplexed into a plurality of output data signals by a phase detector using a plurality of phases of a clock signal, such that each of the output data signals detects an edge or transition in the input data signal and whether the edge or transition is early or late with respect to its corresponding phase of the clock signal.

The Office Action, on the other hand, asserts the following:

> 4. Claims 1-6, 11-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (US Patent No.: 6442225) in view of Baumgartner et al (US Patent No.: 5712580).
>
> a. Claims 1 and 11, Huang discloses a multi-phase voltage controlled oscillator (VCO) accepting a control signal and generates a plurality of multi-phase clock signals for detecting the transition edge of the data signal (Fig. 5, label 24 and

> Abstract, lines 4-7), a phase detector comparing the data signal and clock signals, outputting a plurality of data signals and detecting the transition edge of the data (clock) signal (Fig. 5, label 24 and Col. 1, lines 26-39), a V/I that converter, in the form of a charge pump converts the output from a phase detector and outputs a control current (Fig. 5, labels 22 and Vd) and a loop filter outputting a control signal to the voltage controlled oscillator (Fig. 5, label Vd and 23). Although Huang does not explicitly state an input data signal having a different frequency of the clock signal and retiming/demultiplexing the input dat signal using a phase detector, Baumgartner et al discloses a phase detector, wherein the input data signal is retimed and 1:2 demultiplexed to output data signals, DX and DY, with frequencies 1/2 the frequency of the input data signal. The demultiplexing and retiming is responsive of the clock phase outputted from the VCO (not shown in Daumgartner et al but mentioned in specification) (Fig. 1, labels data, C90, DX, DY, UP and DOWN, Col. 2, lines 39-45, lines 52-60) Based on Huang's invention, Figure 7 shows the components and functionality of the phase detector. One can see that the latches displayed (Fig. 7, labels 212) show the data is latched and D1 and D2 are outputted, which is the same as Fig. 1 disclosed by Baumgartner et al. Thus, it would be obvious to one skilled in the art to determine the functionality of the phase detector disclosed by Huang functions as described by Baumgartner et al based on the similarities found in the diagrams of the phase detector.

Applicants' attorney disagrees. At the indicated locations, Huang and Baumgartner merely describe the following:

> Huang: Fig. 5

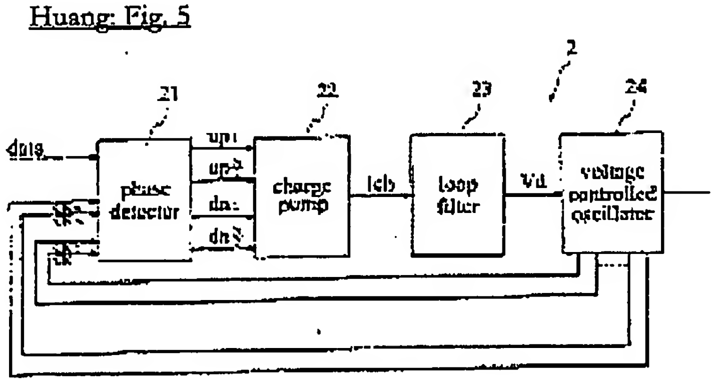

FIG. 5

> Huang: Abstract
>
> The present invention provides a multi-phase-locked loop without dead zone, which can reduce clock jitter and provide larger tolerance for data random jitter. It generates and output multiple sets of control signals (up.sub.k /dn.sub.k) via a multi-phase voltage controlled oscillator which generates a plurality of multi-phase

clock signals for detecting the transition edge of data signal. Therefore, the phase error .theta..sub.e and the voltage Vd of the multi-phase-locked loop can be adjusted to be nearly linear according to the control signals. A multi-phase-locked loop without dead zone thus can be provided.

Huang: Col. 1, lines 26-39 (actually, lines 24-46)

FIG. 1 illustrates a prior art phase-locked loop for data recovery comprising a phase detector 11, a charge pump 12, a loop filter 13, and a voltage controlled oscillator 14. The phase detector 11 is used to receive a data (clock) signal from outside as well as a feedback clock signal CK.sub.vco from the voltage controlled oscillator 14. The phase detector 11 compares the two signals, in accordance with their phase difference .theta..sub.e (.theta..sub.e =.theta..sub.data -.theta..sub.clock), a control signal up or dn will be output to control the charge pump 12. As shown in FIG. 2(a), when the transition edge of the data (clock) signal data leads the falling edge of the feedback clock signal CK.sub.vco, the phase detector outputs an up signal. On the other hand, as shown in FIG. 2(b), when the transition edge of the data (clock) signal data lags behind the falling edge of the feedback clock signal CK.sub.vco, the phase detector 11 outputs a dn signal. The charge pump 12 is controlled by the up and dn control signals output from the phase detector 11 to perform charge/discharge operations, and generates a voltage signal Vd. The loop filter 13 receives the voltage signal Vd and generates an appropriate voltage Vc for controlling the voltage controlled oscillator 14. The voltage controlled oscillator 14 receives the voltage Vc and generates a clock signal CK.sub.vco to be input to the phase detector 11.

Huang: Fig. 7

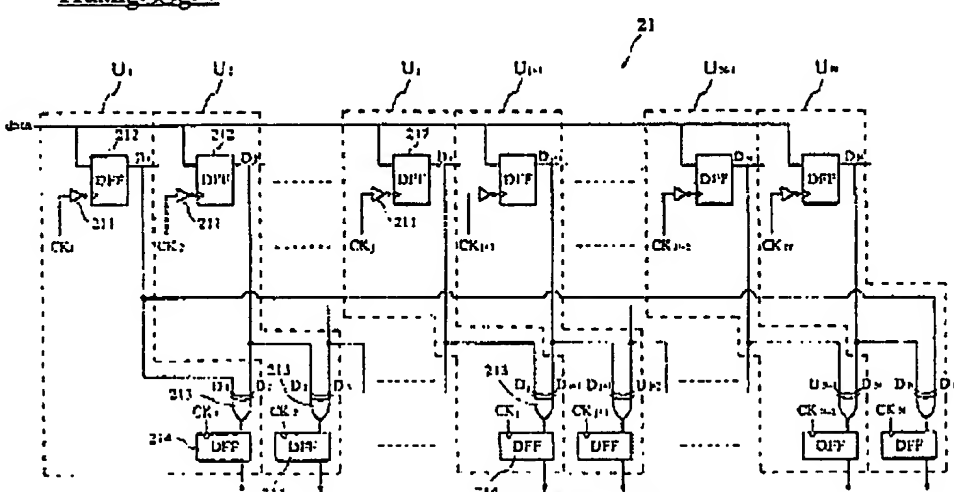

FIG. 7

G&C 30435.179-US-U1

Baumgartner: Fig. 1

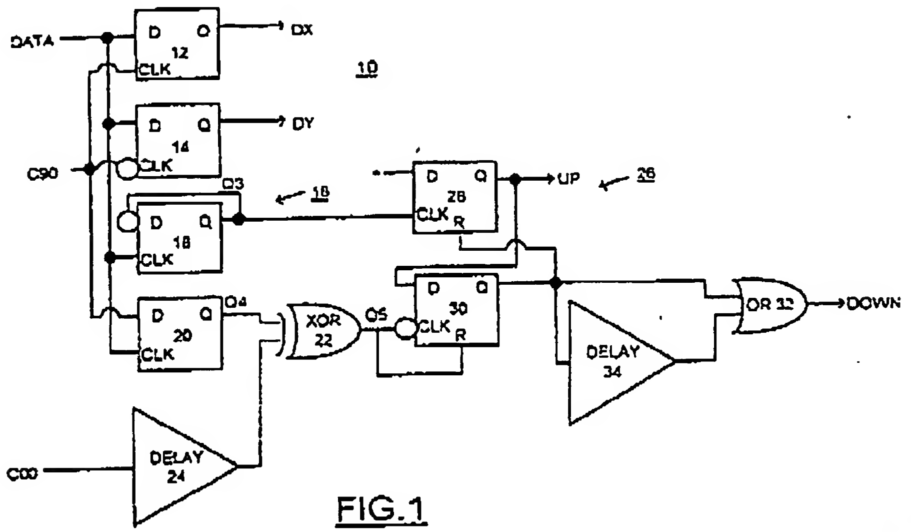

FIG.1

Baumgartner: Col. 2, lines 39-45, lines 52-60 (actually, col. 2, line 34 – col. 3, line 4)

Having reference now to the drawings, FIG. 1 illustrates a linear phase detector in accordance with the invention generally designated by the reference character 10. The linear phase detector 10 is used with a half-speed quadrature clock architecture to phase align to random data. Linear phase detector 10 receives a first half-speed clock signal C00, a second half-speed clock signal C90, and a data signal DATA. The half-speed clock signals C00 and C90 are quadrature signals or clock signal offset by 90 degrees. An oscillator (not shown), such as, a voltage controlled oscillator (VCO) at half the data rate, can be used to generate the half-speed quadrature clock signals C00 and C90.

In accordance with features of the invention, tighter jitter requirements are enabled by the linear phase detector 10 because correction pulses at lines UP and DOWN are only proportional to the phase difference between the clock C00 and DATA signals and are relatively high frequency pulses that are rolled off by a low pass loop filter (not shown) that can be used to adjust the oscillator frequency. Linear phase detector 10 predicts which clock signal edge of the half-speed quadrature clock signal C00 is in-phase with the data edge and then inverts the clock signal C00 (if needed) to generate the correction pulses UP and DOWN accurately.

Linear phase detector 10 includes a pair of retiming latches 12 and 14 that are clocked with the C90 clock signal and perform a 1:2 demultiplexer function on the data signal providing an output DX and DY, respectively. A first clock polarity predicting circuit generally designated by the reference character 16 includes a pair of D-type positive edge triggered flip-flops 18 and 20 and an exclusive OR (XOR) gate 22. To accurately generate an adjusted data signal, the DATA signal is divided down by the first flip-flop 18. First flip-flop 18 is arranged as a divide-by-two with the DATA signal applied to an input CLK of flip-flop 18 and an output Q of flip-flop

> 18 at line Q3 applied to an inverted input D of flip-flop 18. The output Q3 of flip-flop 18 goes high with a first rising edge of the DATA signal and is reset on a next second rising edge of the DATA signal.

The combination of the above portions of Huang and Baumgartner does not teach or suggest that the input data signal is re-timed and de-multiplexed into a plurality of output data signals by a phase detector using a plurality of phases of a clock signal, such that each of the output data signals detects an edge or transition in the input data signal and whether the edge or transition is early or late with respect to its corresponding phase of the clock signal.

For example, the Office Action errs in its characterization of Baumgartner. In Baumgartner, the "demultiplexing" performed by the phase detector, wherein the input data signal is retimed and 1:2 demultiplexed to output data signals, DX and DY, uses only a single phase of the clock, namely C90. Moreover, the output data signals DX and DY are merely complementary values, based on C90 and inverted C90 clocking their respective latches.

In another example, the Office Action errs in its characterization of Huang. In Huang, the signals D1 and D2 in Fig. 7 are "delay" signals, which are used to generate "up" or "down" signals (up_k / dn_k), also referred to as charge/discharge control signals. However, the delay signals of Huang are not a plurality of output data signals that are de-multiplexed by a correspond plurality of phases of a clock signal.

Thus, Applicants' attorney submits that independent claims 1 and 11 are allowable over Huang and Baumgartner. Further, dependent claims 2-10 and 12-20 are submitted to be allowable over Huang and Baumgartner in the same manner, because they are dependent on independent claims 1 and 11, respectively, and because they contain all the limitations of the independent claims. In addition, dependent claims 2-10 and 12-20 recite additional novel elements not shown by Huang and Baumgartner.

IV. CONCLUSION

In view of the above, it is submitted that this application is now in good order for allowance and such allowance is respectfully solicited. Should the Examiner believe minor matters still remain that can be resolved in a telephone interview, the Examiner is urged to call Applicants' undersigned attorney.

Respectfully submitted,

GATES & COOPER LLP
Attorneys for Applicants

Howard Hughes Center
6701 Center Drive West, Suite 1050
Los Angeles, California 90045
(310) 641-8797

Date: November 14, 2005

By: ______________________
Name: George H. Gates
Reg. No.: 33,500

GHG/mrj